UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,665	02/28/2002	George Apostol JR.	31032.P001	2301

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ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No.	**Applicant(s)**
		10/086,665	APOSTOL ET AL.
Office Action Summary		**Examiner**	**Art Unit**	
		Clifford H Knoll	2112 .

-- The MAILING DATE of.this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ . ,

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

     Office Action Summary

DETAILED ACTION

This Office Action is responsive to communication filed 12/27/04. Currently

claims 1-35 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can

be found in a prior Office action.

Claim Rejections - 35 USC § 102

1.   *Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen*

   (US 5197130).

Regarding claims 1 and 10, Chen discloses outbound queues, each of said

outbound bus transactions including a bus arbitration priority (e.g., Fig. 14, "326"); and

a first state machine coupled to the first and second outbound queues to service the first

and second outbound queues, serially requesting for access to the on-chip bus for the

staged outbound bus transactions (e.g., Fig. 14, "322"), according the first queue a first

outbound priority and the second queue a second outbound priority, where access to

the on-chip bus is granted to requesting bus transactions based at least in part on the

included bus arbitration priorities of the contending bus transactions (e.g., col. 17, lines

48-51).

Regarding claims 2 and 11, Chen also discloses a configuration register coupled to said first state machine to store said first and second priorities to be accorded to said first and second outbound queues by said first state machine in servicing said first and second outbound queues (e.g., col. 18, lines 4-9).

Regarding claims 3 and 12, Chen also discloses a third outbound queue, which in conjunction with said first and second outbound queues, facilitates selective staging of a third and said first and second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, with each of the outbound bus transactions including a bus arbitration priority; and said first state machine is also coupled to said third outbound queue, and service said third outbound queue, along with said first and second outbound queues, serially requesting for access to the on-chip bus for the staged outbound bus transactions, according the third queue a third outbound priority complementing said first and second outbound priorities accorded to the first and second outbound queues, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions (e.g., Fig. 19b, "368").

Regarding claims 4 and 13, Chen also discloses inbound queues to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority (e.g., Fig. 14; "324") and a second state machine coupled to the first

and second inbound queues to service the first and second inbound queues, serially

bringing the staged inbound bus transactions to the attention of the on-chip subsystem,

according the first inbound queue a first inbound priority and the second inbound queue

a second inbound priority (e.g., col. 20, lines 51-56).

Regarding claims 5 and 14, Chen also discloses the configuration register

coupled to said second state machine to store said first and second inbound priorities to

be accorded to said first and second inbound queues by said second state machine in

servicing said first and second inbound queues (e.g., Fig. 14, "320").

Regarding claims 6 and 15, Chen also discloses a third inbound queue, which in

conjunction with said first and second inbound queues, facilitates selective staging of a

third and said first and second plurality of inbound bus transactions for the on-chip

subsystem, at the choosing of originating subsystems of the inbound bus transactions,

with each of the inbound bus transactions including a bus arbitration priority, and

granted access to the on-chip bus based at least in part on the included bus arbitration

priority; and said second state machine is also coupled to said third inbound queue,

and service said third inbound queue, along with said first and second inbound queues,

serially bringing the staged inbound bus transactions to the attention of the on-chip

subsystem, according the third queue a third inbound priority complementing said first

and second inbound priorities accorded to the first and second inbound queues (e.g.,

Fig. 19a).

Regarding claims 7 and 17, Chen discloses a first and a second inbound queue

to facilitate selective staging of a first and a second plurality of inbound bus transactions

for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus

transactions, each of the inbound bus transaction including a bus arbitration priority and

being granted access to the on-chip bus based at least in part on the included bus

arbitration priority (e.g., Fig. 19a, "352"); and a state machine coupled to the first and

second inbound queues to service the first and second inbound queues, serially

bringing the staged inbound bus transactions to the attention of the on-chip subsystem,

according the first inbound queue a first inbound priority and the second inbound queue

a second inbound priority (e.g., Fig. 19a, "44").

Regarding claims 8 and 18, Chen also discloses a configuration register coupled

to said state machine to store said first and second inbound priorities to be accorded to

said first and second inbound queues by said state machine in servicing said first and

second inbound queues (e.g., Fig. 14, "320").

Regarding claims 9 and 19, Chen also discloses the third inbound queue (e.g.,

Fig. 19a).

Regarding claims 16 and 20, Chen also discloses selecting one of a memory

controller, a security engine, a voice processor, a collection of peripheral device

controllers, a framer processor, and a network media access controller (e.g., col. 10,

lines 56-66).

Regarding claims 21 and 27, Chen discloses determining intra-subsystem

priorities for transactions with others subsystems of the integrated circuit to be serviced

for requesting access to an on-chip bus of the integrated circuit, to which the

subsystems are coupled (e.g., Fig. 3, "46"); generating and staging the transactions in

accordance with the determined intra-subsystem priorities, including with each of the

staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip

bus with other inter-subsystem transactions of other subsystems of the integrated circuit

(e.g., Fig. 19b); and serially servicing the staged transactions in accordance with their

intra-subsystem priorities, requesting access to the on-chip bus for each staged

transaction being serviced using the included bus arbitration priority (e.g., Fig. 19b,

"362").

Regarding claims 22 and 28, Chen also discloses generating and staging each of

the transactions in a selected one of a plurality of outbound queues in accordance with

the determined intra-subsystem priorities (e.g., Fig. 14, "322"), including with each of the

staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip

bus with other inter-subsystem transactions of other subsystems of the integrated circuit

transactions (e.g., col. 17, lines 48-51).

Regarding claim 23, Chen also discloses staging transactions from other

subsystems in a priority based manner as requested by originating subsystems of the

transactions, each of said transactions from other subsystems having a bus arbitration

priority (e.g., Fig. 14, "322") and serially servicing the staged transactions from other

subsystems, notifying core logic of the subsystem, in accordance with the priority based

manner the transactions from other subsystems are staged (e.g., col. 20, lines 51-56).

Regarding claim 24, Chen also discloses staging each of the transactions from

other subsystems in a selected one of a plurality of prioritized inbound queues as

requested by the originating subsystems of the transactions (e.g., Fig 19a, "352").

Regarding claim 25, Chen discloses staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority (e.g., Fig. 14, "322"), on which access to a on-chip bus the subsystems are coupled was granted; and serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged (e.g., col. 20, lines 51-56).

Regarding claim 26, Chen also discloses staging each of the transactions from other subsystems in a selected one of a plurality of prioritized inbound queues as requested by the originating subsystems of the transactions (e.g., Fig 19a, "352").

Regarding claims 29 and 30, Chen also discloses the inbound queues to facilitate selective staging of a first and a second plurality of inbound bus transactions for core logic of the particular subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transaction including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority (e.g., Fig. 14, "326"); and a second state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the core logic of the particular subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority (e.g., col. 17, lines 48-51).

Regarding claim 31, Chen also discloses selecting one of a memory controller, a

security engine, a voice processor, a collection of peripheral device controllers, a framer

processor, and a network media access controller (e.g., col. 10, lines 56-66).

Regarding claim 32, Chen discloses first and second subsystems each having a

data transfer interface initiating transactions with other subsystems through selective

employment of facilities of the data transfer interface to internally prioritizing the order

the transactions are to be serviced by the data transfer interface (e.g., Fig 19b), and

including with said first transactions first bus arbitration priorities to facilitate prioritization

of granting of access to the on-chip bus to contending inter-subsystem transactions

including said first transactions (e.g., col. 17, lines 48-51).

Regarding claim 33, Chen also discloses the first data transfer interface of the

first subsystem staging third transactions from other subsystems in a priority based

manner as requested by originating subsystems of the third transactions, said third

transactions from other subsystems also having third bus arbitration priorities, based on

which accesses to said on-chip bus were granted (e.g., Fig 19a, "44").

Regarding claim 34, Chen also discloses the first data transfer interface of the

first subsystem serially servicing the staged third transactions from other subsystems,

notifying core logic of the first subsystem, in accordance with the priority based manner

the third transactions from other subsystems are staged (e.g., Fig 19a, "44").

Regarding claim 35, Chen also discloses the second data transfer interface of

the second subsystem staging fourth transactions from other subsystems in a priority

based manner as requested by originating subsystems of the fourth transactions, said

fourth transactions from other subsystems also having fourth bus arbitration priorities,

based on which accesses to said on-chip bus were granted (e.g., Fig 19a, "44").

Response to Arguments

Applicant's arguments filed 12/27/04 have been fully considered but they are not

persuasive.

Applicant argues that Chen does not disclose "a second outbound data queue,

much less mention a state machine to accord a first queue a first outbound priority and

a second queue a second outbound priority" (p. 12); however, the cited Figure shows a

queue (Fig. 14, "326"). For the particular feature of the second outbound data queue,

the supporting specification notes in "FIG. 14, a pair of similar arbitration networks 320

and 322 is shown for one of the memory ports 310 and one of the processor ports 308.

It will be recognized that similar circuitry is replicated for each of the memory ports 310

and the MRCA port 312, and for each of the ports 302, 304, 306 and 308 connected to

the processors 100. As explained in further detail hereinafter, the arbitration networks

320 and 322 use a first-come-first-served, multiple-requestor-toggling system to insure

that the oldest reference is processed first. In the case of multiple old references of the

same age, a fairness algorithm ensures equal access to the ports connected to that

arbitration network 320 or 322" (col. 17, lines 30-43). Thus, Examiner finds these

features disclose multiple outbound queues and its consequent arbitration.

Applicant further argues that Chen does not disclose "each of the outbound bus transactions will include a bus arbitration priority, as required by claim 1, for example. The data queue 326 in Chen is a simple first-in-first-out (FIFO) queue that bases priority on time of reception" (p. 4); however, this "priority on time of reception" scheme, as put by the Applicant, is a valid prioritization scheme for an arbitrator; if the Applicant intends a particular prioritization scheme to distinguish from this time of reception prioritization, then it must be positively recited. Any distinguishing recitation should note however, the fairness algorithm scheme that is taught by Chen as cited supra in the passage supporting the interpretation of Figure 14.

Applicant further argues that Chen does not disclose a bus; however the "I/O CHANNEL" features of Figure 14 which link the arbitration node ("44") with the processors are interpreted as buses.

Regarding claim 7, Applicant argues that Chen does not disclose "a first inbound queue and a second inbound queue to facilitate staging of transactions from an on-chip bus to an on-chip subsystem", and argues that, in distinction to the claimed invention, Chen's "queues 352 are found on dedicated lines that provide point-to-point access between the arbitration node of the MRCA and the respective external NRCA" (p. 13); however, while the queues are involved in queuing external data which arrives at the arbitration circuit on a separate bus, upon the result of an arbitration, they are placed on an on-chip bus. For these particular details, Figure 14, "ADDR/DATA" and its output bus (as mediated by "320", providing "ADDR/DATA (SECTION PATH)" to other circuits) are considered adequate disclosure of an on-chip bus.

Applicant further argues that Chen's queues are "FIFO based queues and have no priority distinction"; however, as stated supra, FIFOs instantiate a time of reception priority scheme, and to further distinguish, Chen additionally teaches a fairness algorithm scheme (quoted supra) that works in concert with the time of reception scheme.

Regarding claim 21, Applicant argues that Chen does not disclose an "on-chip bus"; however, this argument has been treated supra. Applicant further argues that Chen does not disclose "subsystems of an integrated circuit", and argues that in distinction Chen has "no suggestion that any of the components reside on the same chip"; however the recitation does not support the distinction of the same chip, rather, an "integrated circuit" is recited. Nonetheless, the cited feature in the figure (Fig. 3, "46") is part of an integrated circuit that constitutes subsystems. Although the subsystems are subsequently connected to external elements (via "58"), this does not preclude their interpretation as subsystems.

Regarding claim 27, Applicant argues that Chen does not disclose an "on-chip bus"; however, this argument has been treated supra. Applicant further argues that Chen does not disclose "a data transfer interface to initiate transactions with other subsystems (also coupled to the on-chip bus) in a prioritized manner", and distinguishes Chen as "simply receiv[ing] requests from internal arbitration nodes into respective queues" (p. 16); however, the ordering performed by the queue (i.e., a FIFO arrangement) is a priority scheme, further augmented by a fairness algorithm, as discussed supra.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Clifford H Knoll whose telephone number is 571-272-

3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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you have questions on access to the Private PAIR system, contact the Electronic

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chk

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